Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently Amended) A method of operating a data-processing device with an integrated circuit comprising ~~a central processing unit (CPU) and~~ one or more ~~co-processors~~processors ~~,~~ ; in which the integrated circuit performs cryptographic operations, the method comprising:

~~in~~ performing cryptographic operations in the integrated circuit, wherein at least ~~two processors, CPU and co-processors,~~two of the one or more processors perform the cryptographic operations simultaneously and in parallel,

wherein the cryptographic operations of at least one ~~processor~~of the one or more processors ~~,~~ ~~CPU or co-processor,~~ are useful operations and the cryptographic operations performed by at least one other processor~~, CPU or co-processor,~~ are dummy operations whose results are rejected, and wherein the selection as to which of the one or more processors~~, CPU or co-processor,~~ performs a useful operation is randomly controlled, and

wherein consumption characteristics of the data-processing device being a superimposition of consumption characteristics associated with performing both useful and rejected cryptographic operations, whereby reconstruction of the consumption characteristics associated with performing any of the useful cryptographic operations is impeded.

3. (Currently Amended) A method as claimed in claim 2, wherein the one or more processors comprise a CPU and at least one co-processor ~~selection as to which processor, CPU or co-processor, performs a useful operation is random-controlled.~~

4. (Currently Amended) A method as claimed in claim 2, wherein a cryptographic operation is split up into at least two sub-operations and at least one of the at least two sub-operations is a useful operation and at least one of the at least two sub-operations is a dummy operation. ~~at least two processors perform at least one sub-operation in parallel and simultaneously with at least one dummy operation.~~

5. (Canceled)

6. (Canceled)

7. (Previously Presented) A method as claimed in claim 4, wherein subsequently corresponding sub-results from the respective sub-operations are combined to an overall result of the overall cryptographic operation.

8. (Currently Amended) A method as claimed in ~~claim 7~~claim 4, ~~characterized in that~~wherein the split-up of the cryptographic operation into sub-operations is ~~random~~randomly controlled.

9. (Previously Presented) A method as claimed in claim 7, characterized in that the sub-operations are parts of an encryption in accordance with Data Encryption Standard (DES).

10. (Currently Amended) A data-processing device with an integrated circuit, comprising:

~~a central processing unit (CPU) and one or more co-processors~~one or more processors, a control unit which controls the ~~CPU and co-processors~~one or more processors so that, in the case of a cryptographic operation, the ~~at least two of the CPU and co-processors~~one or more processors perform a cryptographic operation simultaneously and in parallel with at least one dummy operation, and wherein the selection as to which of the one or more processors performs a useful operation is randomly controlled,

whereby consumption characteristics associated with performing the respective cryptographic and dummy operations are superimposed so that reconstruction of the consumption characteristics associated with performing the cryptographic operation is impeded.

11. (Currently Amended) A data-processing device as claimed in claim 10, wherein the control unit comprises a splitter which splits a cryptographic operation into at least two sub-operations, and at least one of the at least two sub-operations is a useful operation and at least

one of the at least two sub-operations is a dummy operation. ~~and at least one dummy operation is supplied for simultaneous processing to two separate of the CPU and co-processors.~~

12. (Currently Amended) A data-processing device as claimed in claim 11, wherein the control unit further comprises a recombiner which recombines each sub-result of the sub-operations simultaneously performed and wherein ~~by the CPU and co-processors and~~ the at least one dummy operation results are rejected to produce an overall result of the overall cryptographic operation.

13. (Currently Amended) A data-processing device as claimed in claim 12, ~~wherein the splitter splits a cryptographic operation so that at least one sub-operation is a dummy operation, and~~ wherein the recombiner rejects the relevant result of ~~a~~ the at least one processor of the one or more processors ~~processor~~ that ~~has~~ performed such dummy operation.

14. (Currently Amended) A data-processing device as claimed in claim ~~13~~10, wherein the one or more processors comprise a CPU and at least one co-processor. ~~further comprising a random generator which is connected to the splitter so that the splitter operates in a random-controlled manner~~.

15-28. (Canceled)